

Recently the computer industry has discovered the advantages of 2½D memories. It's real excited about the speed of linear select memories, coupled with considerably lower drive and selection circuitry costs. And every memory manufacturer is rushing to get on the bandwagon.

Indiana General is already sitting there. 2½D stacks are old hat to us. And we don't mean prototypes. We've been designing, building and delivering 2½D stacks for mili-

tary, industrial and commercial applications for over a year. Including both two and three wire 2½D memories.

We'll be glad to send you complete details on 2½D stacks . . . including delivery dates. In addition to 2½D stacks we can offer a lot more choices. Including: 2D and 3D stacks; printed circuit, molded, or pluggable molded planes; and the IGC-developed folded-array Microstack®.

Staying up front in the memory field is a

habit with us. It started when we invented memory cores and our accomplishment in 2½D stacks keeps us in the driver's seat. So if you want something new in memory stacks, drop us a line. It, too, may be old hat with us. Write Mr. Thomas Loucas, Manager of Sales, Indiana General Corporation, Electronics Division/Memory Products, Keasbey, New Jersey.

INDIANA GENERAL 

**2½D stacks are already
old hat to Indiana General**





FERRAMIC® MEMORY CORE SPECIFICATION SUMMARY

The core types listed below are currently in production and readily available.

For price and delivery information on core types not listed, please contact the Memory Product sales department, Keasbey, New Jersey, phone (201) 826-5100.

PART NO.	Memory Cycle Time	SIZE CLASS (O.D.)	Test Currents (ma)	Tr (usec)	Td (usec)	Min μV_1 (mv)	Max dV_z (mv)	Temp. = 24°C ± 1 Freq. = 10Kc	
								Tp (usec)	Max Ts (usec)
MC-184	<1	20 mil	640/385	0.05	0.5	35	9	0.10 ± 0.02	0.25
MC-917*	1	20 mil	820/500	0.05	0.5	42	13	0.11 ± 0.02	0.26
MC-919*	1-2	20 mil	700/435	0.05	1.0	35	10	0.15 ± 0.03	0.35
MC-190	1-1.5	30 mil	750/458	0.10	1.0	52	10	0.18 ± 0.03	0.34
MC-181	1.5	30 mil	650/400	0.10	1.5	46	9	0.23 ± 0.03	0.45
MC-188*	1.5	30 mil	700/420	0.10	1.0	42	10	0.26 ± 0.04	0.60
MC-189	2	30 mil	520/323	0.10	1.0	42	10	0.24 ± 0.03	0.46
MC-908	2	30 mil	450/275	0.05	1.5	34	17	0.19 ± 0.03	0.45
MC-183*	3-5	30 mil	600/360	0.10	1.0	34	10	0.32 ± 0.04	0.70
MC-179	4-5	50 mil	460/275	0.20	2.0	60	12	0.45 ± 0.05	0.95
MC-138	5-6	50 mil	450/285	0.20	2.0	45	9	0.56 ± .05	1.25
MC-140	5-6	50 mil	400/245	0.20	2.0	50	11	0.58 ± .05	1.25
MC-227*	5-6	50 mil	700/424	0.50	2.5	52	8	0.78 ± 0.05	1.35
MC-149	6-8	50 mil	320/195	0.50	5.0	38	6	0.88 ± .10	1.6
MC-113	5-6	80 mil	740/475	0.20	2.0	100	30	0.56 ± 0.5	1.3
MC-142	8-10	80 mil	360/220	0.50	6.0	42	10	1.5 ± .05	2.9

*Wide Temperature

Detail Memory Core — Specification Sheets On All Above Part Numbers Available On Request



20 MIL

FERRAMIC® MEMORY CORE SPECIFICATION

260 NANOSECOND SWITCHING MATERIAL, WIDE TEMPERATURE RANGE

PART NO. MC 917

This specification supersedes all preliminary engineering bulletins covering this part

DIMENSIONS:

Outer Diameter = $0.023'' \pm 0.001''$
 Inner Diameter = $0.014'' \pm 0.001''$
 Height = $0.006'' \pm 0.001''$

DEFINITIONS:

All terms used in this specification are defined on the reverse side.

GENERAL:

This specification describes a 260 nanosecond switching material in the 20 mil size, for magnetic cores to be used in a very high speed coincident current memory.

The cores are available at the following quality level.
 MC 917 Shipped to .015 AQL

MIL Standard 105 D inspection level II is used for sampling.

RE: A.S.T.M. C-526-63T

"Tentative method of test for non-metallic magnetic cores to be used in a coincident current memory with a two-to-one selection ratio operating under full switching conditions"

ELECTRICAL:

Each lot is inspected to the following electrical specifications:

Temperature $24^{\circ} \text{C.} \pm 1^{\circ} \text{C.}$

Current Drive Pulse

$I_{\text{read}} = I_{\text{write}} = 820 \text{ milliamperes} \pm 1\%$
 $I_{\text{partial write}} = 500 \text{ milliamperes} \pm 1\%$
 $t_r = 50 \text{ nanosecond (linear)}$
 $t_d = 500 \text{ nanosecond}$

All cores are tested using the pulse sequence shown in Figure 4 on the reverse side.

The Undisturbed ONE Voltage Output

μV_1 equal to or greater than 42 millivolts
 at measuring time $t_m = 0.11 \mu\text{sec.}$

The Disturbed ZERO Voltage Output

dV_z not greater than 13 millivolts (peak)

Switching Time

T_s equal to or less than 260 nanosecond

Peaking Time

T_p equal to 110 nanosecond ± 20 nanosecond

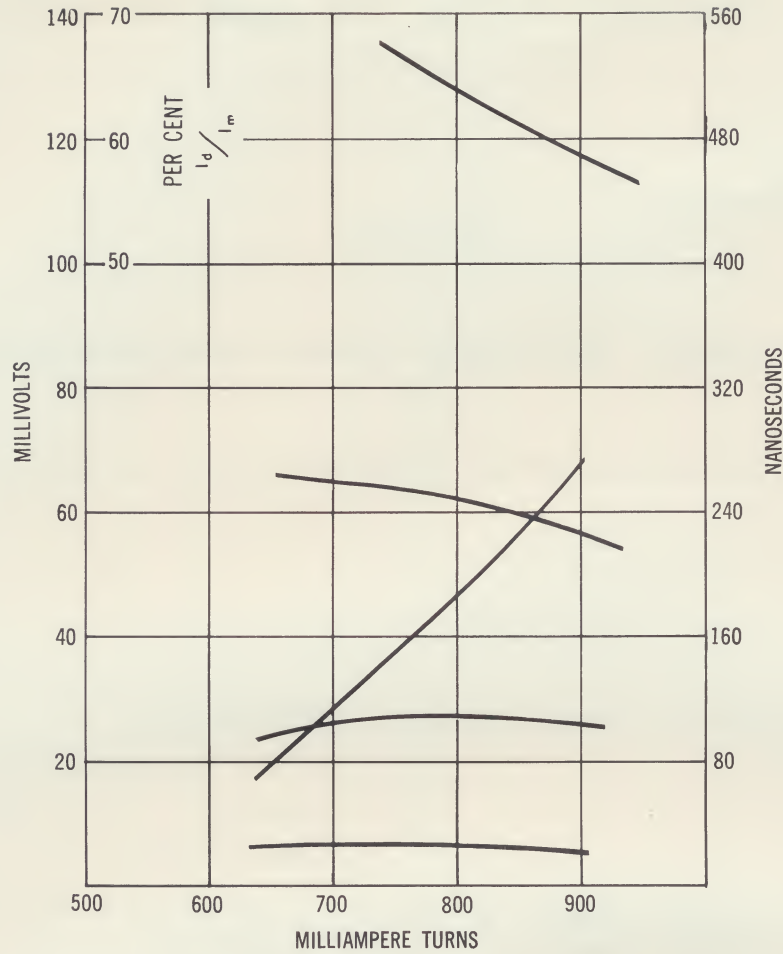
MECHANICAL:

All cores subjected to mechanical testing must pass for the lot to be accepted.

The physical dimensions are checked on a random sample.

Broken cores are not to be counted as rejects during incoming inspection.

FIGURE 1 Typical Characteristics at 25°C



CURRENT PULSE

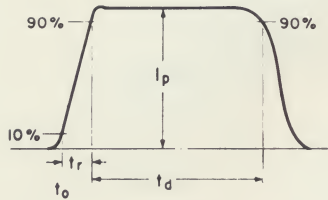


Figure 2

VOLTAGE RESPONSE

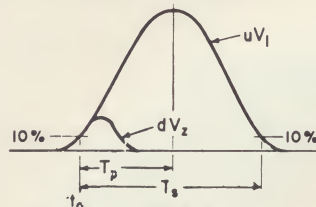


Figure 3

CURRENT PULSE SEQUENCE

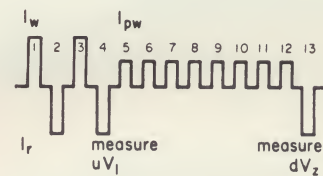


Figure 4

I_p —The peak amplitude of the current pulse.
 t_o —The reference timing point on the rise of the current pulse designated as 10% of the peak amplitude (I_p).
 t_r —The rise time of the current pulse from 10% of peak amplitude (t_o) to 90% of peak amplitude.
 t_d —The pulse duration from 90% on the rise to 90% on the fall of the peak amplitude.
The current pulse, illustrated in Figure 2, must have the following characteristics;
The rise time, t_r , must be linear.
The droop in the flat portion must be less than 1%.
The over-shoot must be less than 1%.

uV_1 —The selected undisturbed ONE voltage output.
 dV_z —The selected disturbed ZERO voltage output resulting from partial write pulses only.
 T_p —The peaking time of the undisturbed ONE voltage output (uV_1) referred to t_o on the voltage response.
 T_s —The memory core switching time measured from t_o on the rise of the undisturbed voltage response (uV_1) to 10% on the fall of the uV_1 voltage response.
 t_o —The 10% amplitude reference timing point on the rise of the voltage response.
A typical voltage pulse response is illustrated in Figure 3.

The current pulse sequence used for the yield evaluation in this specification and for 100% inspection is shown in Figure 4.
The basic pulse repetition frequency, defined as the reciprocal of the time interval between two consecutive pulses, is 10 KC or less.
The following symbols are used to define the directions of the current pulses shown in Figure 4.

I_w —Write pulse
 I_{pw} —Partial write pulse
 I_r —Read pulse

Ferramic® Memory Cores are available as complete assemblies in a standard line of Planes and Stacks including the new line of Printed Circuit assemblies. 100% testing and quality assurance procedures are employed throughout the manufacturing process. Request additional information about the standard line of Planes and Stacks giving your application requirements.



20 MIL

FERRAMIC® MEMORY CORE SPECIFICATION

340 NANOSECOND SWITCHING MATERIAL, WIDE TEMPERATURE RANGE

PART NO. MC 919

This specification supersedes all preliminary engineering bulletins covering this part

DIMENSIONS:

Outer Diameter = $0.0230'' \pm 0.001''$
 Inner Diameter = $0.014'' \pm 0.001''$
 Height = $0.006'' \pm 0.0005''$

DEFINITIONS:

All terms used in this specification are defined on the reverse side.

GENERAL:

This specification describes a 340 nanosecond switching material in the 20 mil size, for magnetic cores to be used in a very high speed coincident current memory.

The cores are available at the following quality level.

MC 919 Shipped to .015 AQL

MIL Standard 105 D inspection level II is used for sampling.

RE: A.S.T.M. C-526-63T

"Tentative method of test for non-metallic magnetic cores to be used in a coincident current memory with a two-to-one selection ratio operating under full switching conditions"

ELECTRICAL:

Each lot is inspected to the following electrical specifications:

Temperature $24^{\circ} \text{C.} \pm 1^{\circ} \text{C.}$

Current Drive Pulse

$I_{\text{read}} = I_{\text{write}}$	= 700 milliamperes $\pm 1\%$
$I_{\text{partial write}}$	= 435 milliamperes $\pm 1\%$
t_r	= 50 nanosecond (linear)
t_d	= 1.0 microsecond

All cores are tested using the pulse sequence shown in Figure 4 on the reverse side.

The Undisturbed ONE Voltage Output

uV_1 equal to or greater than 35 millivolts at peak.

The Disturbed ZERO Voltage Output

dV_z not greater than 10 millivolts (peak)

Switching Time

T_s equal to or less than 340 nanosecond

Peaking Time

T_p equal to 150 nanosecond ± 30 nanosecond

MECHANICAL:

All cores subjected to mechanical testing must pass for the lot to be accepted.

The physical dimensions are checked on a random sample.

Broken cores are not to be counted as rejects during incoming inspection.

CURRENT PULSE

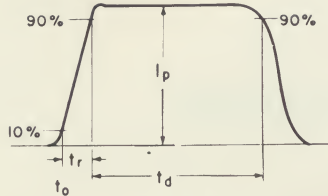


Figure 2

VOLTAGE RESPONSE

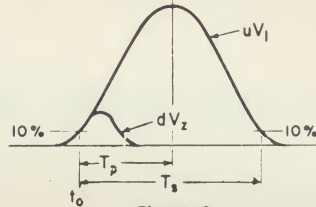


Figure 3

CURRENT PULSE SEQUENCE

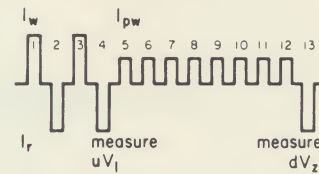


Figure 4

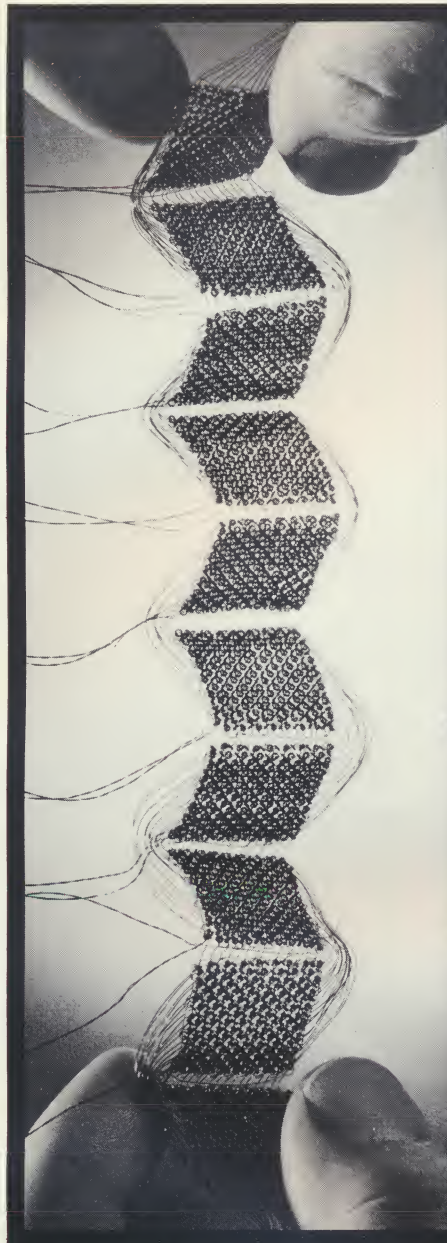
I_p —The peak amplitude of the current pulse.
 t_o —The reference timing point on the rise of the current pulse designated as 10% of the peak amplitude (I_p).
 t_r —The rise time of the current pulse from 10% of peak amplitude (t_o) to 90% of peak amplitude.
 t_d —The pulse duration from 90% on the rise to 90% on the fall of the peak amplitude.
The current pulse, illustrated in Figure 2, must have the following characteristics:
The rise time, t_r , must be linear.
The droop in the flat portion must be less than 1%.
The over-shoot must be less than 1%.

uV_1 —The selected undisturbed ONE voltage output.
 dV_z —The selected disturbed ZERO voltage output resulting from partial write pulses only.
 T_p —The peaking time of the undisturbed ONE voltage output (uV_1) referred to t_o on the voltage response.
 T_s —The memory core switching time measured from t_o on the rise of the undisturbed voltage response (uV_1) to 10% on the fall of the uV_1 voltage response.
 t_o —The 10% amplitude reference timing point on the rise of the voltage response.
A typical voltage pulse response is illustrated in Figure 3.

The current pulse sequence used for the yield evaluation in this specification and for 100% inspection is shown in Figure 4.
The basic pulse repetition frequency, defined as the reciprocal of the time interval between two consecutive pulses, is 10 KC or less.
The following symbols are used to define the directions of the current pulses shown in Figure 4.

I_w —Write pulse
 I_{pw} —Partial write pulse
 I_r —Read pulse

Ferramic® Memory Cores are available as complete assemblies in a standard line of Planes and Stacks including the new line of Printed Circuit assemblies. 100% testing and quality assurance procedures are employed throughout the manufacturing process. Request additional information about the standard line of Planes and Stacks giving your application requirements.



we probed
miniaturization



HIGHER RELIABILITY
GREATER BIT DENSITY
LOWER COST



microstack*

IGC's folded array memory stack . . . commercial, industrial and military

INDIANA GENERAL 

ELECTRONICS DIVISION / MEMORY PRODUCTS

KEASBEY, NEW JERSEY

microstack® - miniaturized, folded array memory stack

HIGHER RELIABILITY, GREATER BIT DENSITY, LOWER COST

Indiana General's modular Microstack design utilizes the folded array technique of stringing cores. This unique method of stack construction was pioneered by IGC and has been time-proven in hundreds of systems.

Reliability is built right into IGC Microstacks. In the folded array technique, mats of cores are strung on *continuous* wires, and then folded one upon the other to form the complete array for a stack module. This method reduces the number of solder connections by 80%, compared to conventional frame construction. For example, in a stack of 4000 words and 10 bits, the Microstack has 2500 fewer solder joints than a standard stack. The reduction in solder joints means an increase in product reliability.

UP TO 90% SMALLER

The elimination of frames normally required for support of individual mats results in an extremely compact package . . . up to 90% smaller than conventional memory stacks.

The Microstack's lower cost is due to the elimination of frames, reduced number of solder connections and a consequent reduction of rework.

UNLIMITED BIT LENGTH AND WORD SIZE

The physical configuration of the Microstack's windings are the same as for a conventional memory plane; therefore, the electrical characteristics of both types are virtually identical. Individual Microstack modules can be stacked to achieve any desired bit length. Like conventional frame wiring, word size

Memory frames are eliminated in the Microstack. Individual cores are aligned with one another in a jig and all wiring is strung continuously with unbroken wires.



I.G.C. folded array Microstacks have up to 80% fewer solder joints, consequently greater reliability.

is also flexible so as to meet specific requirements of virtually any application.

THREE PACKAGES . . . FOR COMMERCIAL, INDUSTRIAL AND MILITARY APPLICATIONS

In developing the complete Microstack line, IGC engineers gave special consideration to the three broad system application categories, commercial, industrial and military.

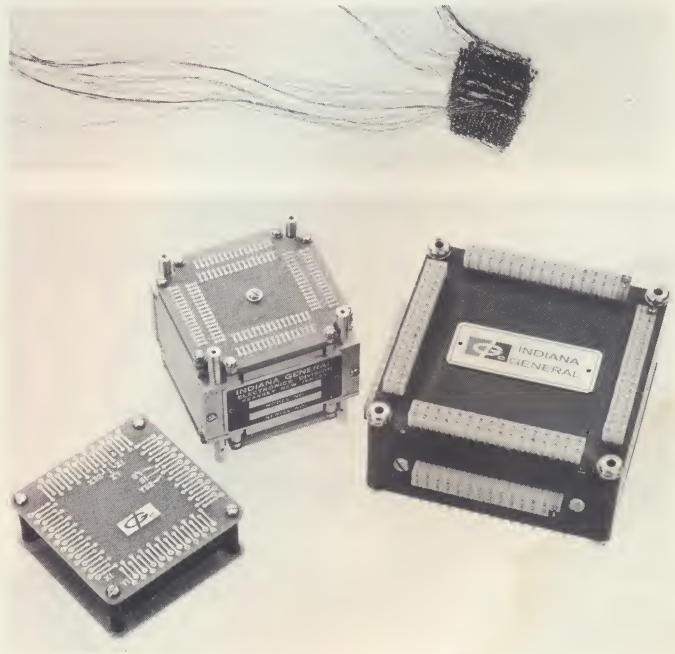
The commercial Microstack uses top and bottom printed circuit frames for interconnection to the memory system. The Ruggedized Microstack for such industrial applications as process control, meets light shock and vibration specifications. Built-in connectors are provided for memory expansion by plugging one stack into another.

RUGGED CONSTRUCTION MEETS MILITARY AND N.A.S.A. REQUIREMENTS

The most recent type of Microstack, developed for military aerospace applications, is designed to meet the most rugged military and N.A.S.A. requirements while still providing low cost and important size and weight advantages. These militarized Microstacks can be designed to operate reliably in extremes of temperature, humidity, altitude, vibration, shock and corrosive environments. In addition they offer simplified servicing and ease of expansion.

The Microstack concept is available either as a standard IGC off-the-shelf product or as a solution to a specific design problem through the use of IGC's Memory Products Engineering Department. No matter what your needs, the chances are that the Microstack is your answer.

The entire mat is then removed and the matrices are folded one upon the other.



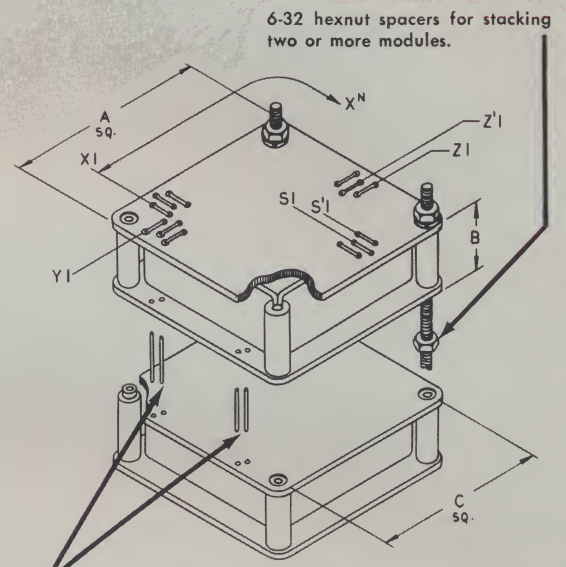
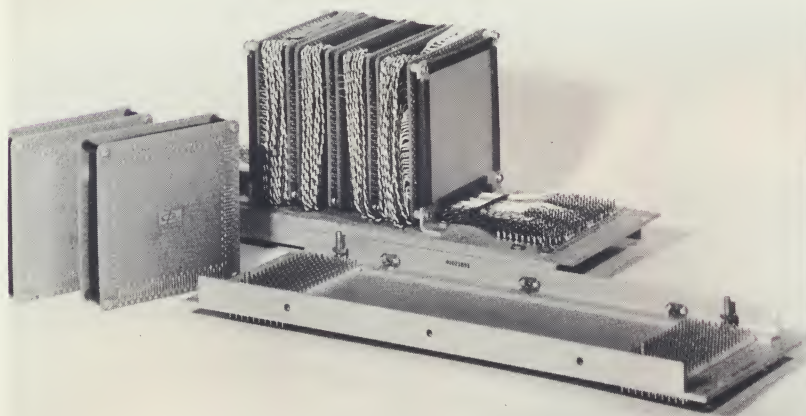
Microstacks are available in a wide range of packages for applications in commercial, industrial and military systems.

commercial applications

The first Microstack was introduced by IGC for commercial applications. Top and bottom printed circuit boards serve as the means by which individual commercial Microstacks are stacked to form the desired bit length. The "x" and "y" drive line of two or more modules are connected in series by means of pins soldered between terminals, thereby eliminating external jumpers.

An indication of the unit's high reliability and quality standards is the fact that typical IGC commercial Microstacks containing over 32,000 cores have passed such vibration and shock tests as MIL-T4708.

64 x 64 x 30 Microstack for commercial applications

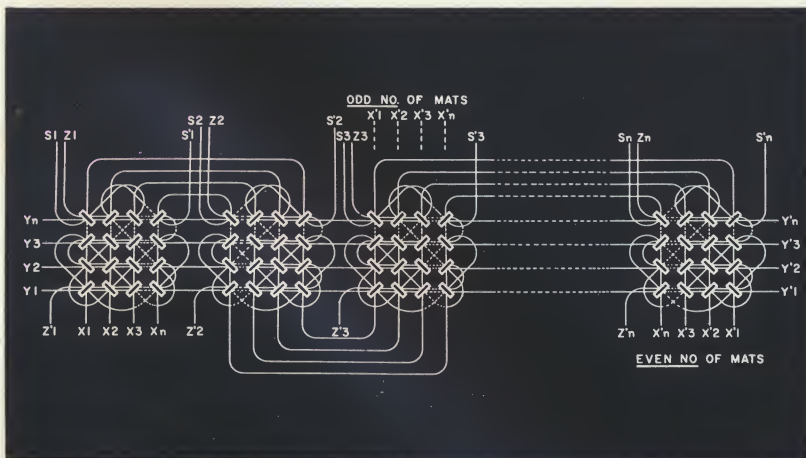


The "x" and "y" drive lines of two or more modules are connected in series by means of pins, soldered between terminals, thereby eliminating the need for external jumpers.

SPECIFICATIONS — STANDARD COMMERCIAL MICROSTACKS

Other sizes available to meet your specific needs.

Maximum Array .030 and .050 Cores	Dimensions			Approx. Weight
	A	B	C	
16x16x8	2.350	1.187	1.950	3 oz.
32x32x8	3.150	1.187	2.750	6 oz.
64x64x8	4.750	1.187	4.350	10 oz.



MEMORY OPERATING INSTRUCTIONS

"Yn" & "Xl" drive current shall be in phase and equal in amplitude.

The drive current for odd numbered "X" drive lines shall be of the same polarity as "Xl".

The drive current for even numbered "X" drive lines shall be opposite polarity as "Xl".

The drive current for odd numbered "Y" drive lines shall be of the same polarity as "Yl".

The drive current for even numbered "Y" drive lines shall be opposite polarity as "Yl".

"ZI" (inhibit winding) drive current shall be opposite in polarity to the "Yn" drive current.

"SI" & "S'l" (sense winding) on which both plus and minus core outputs appear.

"Yn" & "Xl" core is always oriented as shown for any size array.

industrial applications

INSTANT EXPANSION

A growing number of memory system applications require expandable storage capacity. To meet these requirements, Indiana General developed the Industrial Microstack — a tough, compact new memory stack with built-in connectors allowing instant expansion of memory system bit length.

PLUGGABLE EXPANSION

With IGC's connector-type Microstack modules, memory capacity can be doubled, tripled, quadrupled, etc. in a matter of minutes.

A complete memory for a particular application is composed of one or more Microstack modules, each with a standard length up to fourteen bits. Modules are standardized in 16x16, 32x32, and 64x64 arrays, with special variations available if required. All leads of each individual module are terminated with connectors mounted directly onto the enclosure. The X and Y drive lines start and finish on opposite ends

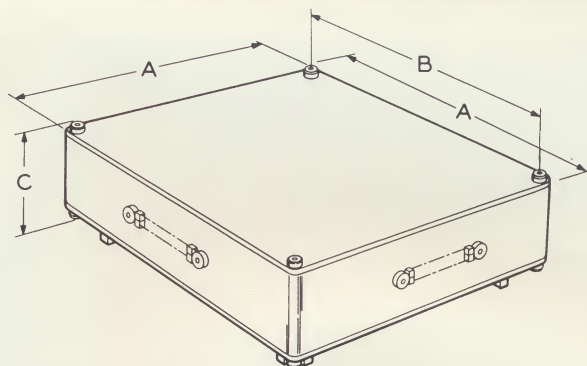
of the module; one end a male connector, the other a female connector. Sense and inhibit connectors are located in the sides. This unique design permits modules to be plugged together "piggyback" to form a stack of any desired bit length. A memory stack can be expanded in a matter of minutes by simply adding a sense and inhibit connector to the memory system. For example, two 64x64x10 Microstack modules, plus 10 minutes will yield a size 64x64x20 memory stack similar to the photograph shown lower left.

CONNECTOR DESIGN

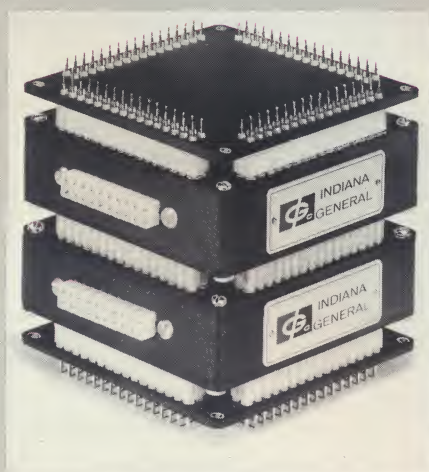
The connectors used in this Microstack are designed for wire wrap; however, internal connections are soldered due to the small gauge wire necessary in core matrices. Mating connectors for external circuitry can be offered suitable for wire-wrap, or with shortened posts suitable only for soldering. These connectors can be shipped in advance for prewiring into the system so that the unit will be ready to accept the stack when it is delivered.

SPECIFICATIONS—STANDARD INDUSTRIAL MICROSTACK. Other sizes available to meet your specific needs.

MAXIMUM ARRAY	MODULE DIMENSIONS		
	A	B	C
30 Mil Cores			
16x16x10	1.734	1.296	1 $\frac{1}{16}$
32x32x10	2.218	1.781	1 $\frac{1}{4}$
64x64x10	3.187	2.750	1 $\frac{1}{2}$
50 Mil Cores			
16x16x10	2.343	1.906	1 $\frac{7}{32}$
32x32x10	3.156	2.718	1 $\frac{15}{32}$
64x64x10	4.750	4.312	1 $\frac{27}{32}$
80 Mil Cores			
16x16x10	2.828	2.390	2 $\frac{1}{32}$
32x32x10	4.109	3.671	2 $\frac{1}{32}$
64x64x10	6.671	6.234	2 $\frac{1}{32}$



Standard connector plates, included on top and bottom of stack increase overall height (dimension "C") by approximately $\frac{1}{8}$ ".



64 x 64 x 14 Ruggedized Microstack for industrial applications.

The Microstack for industrial applications meets many military environmental specifications including the vibration test illustrated.



IGC MICROSTACKS MEET MANY MIL. SPECS.

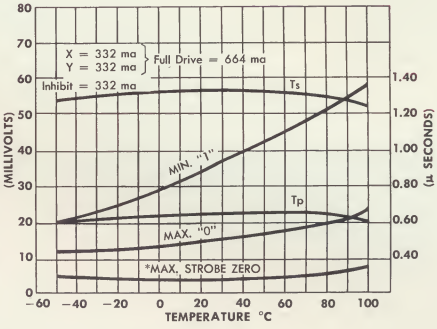
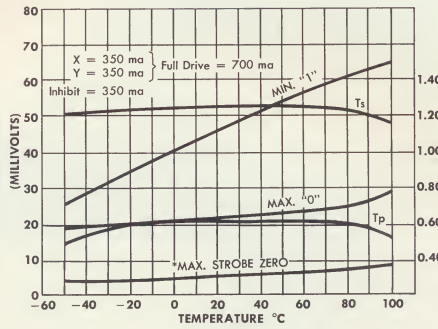
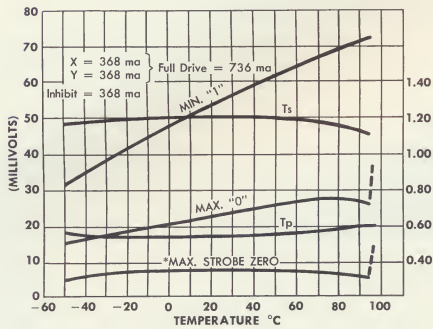
IGC's Industrial Microstack will meet extreme environmental tests in compliance with the following military specifications:

Vibration — MIL-E-5272C, proc. XII.

Humidity — MIL-T-5422E, para. 4.4.

Altitude — MIL-E-5272C, cond C.

Shock — MIL-E-5272C, proc. V, using MIL-S-4456 (sand drop) and MIL-E-5272C, proc. V, using MIL-S-901 (hammer).

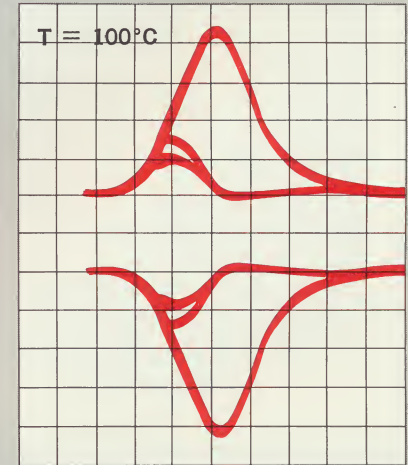
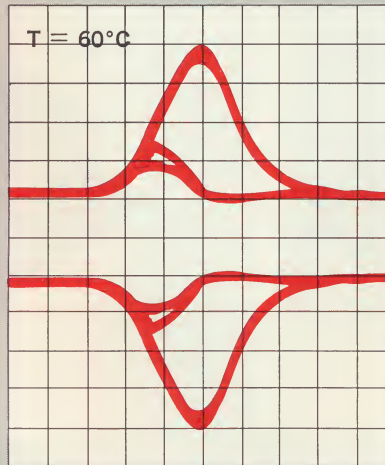
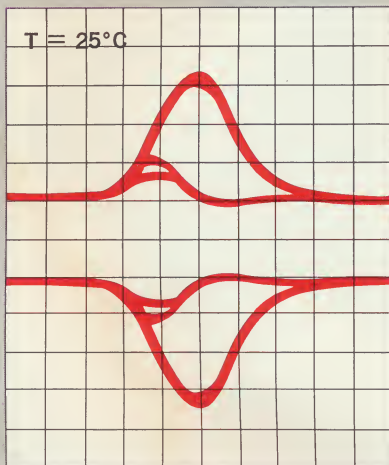
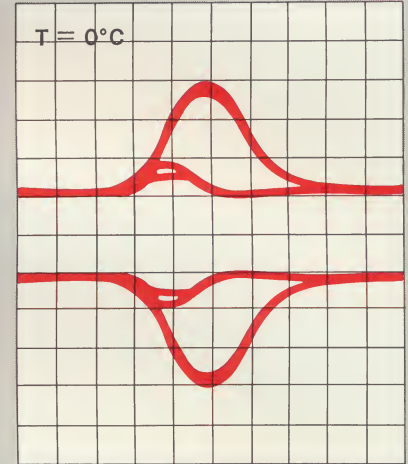
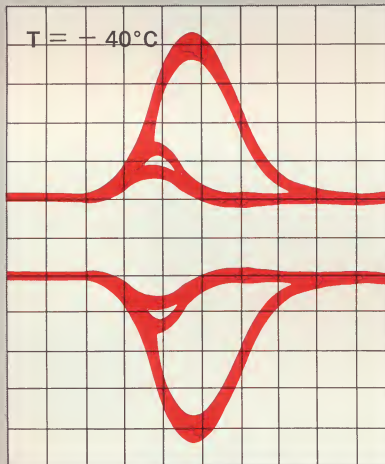


Typical data for 64 x 64 Microstack mat using 50 mil., wide temperature cores.

64x64x10 INDUSTRIAL MICROSTACK. DOUBLE CHECKERBOARD PATTERN.

I Read-Write = 700 ma
I Inhibit = 350 ma
 T_r = 0.30 μ S
 T_d = 1.5 μ S

SCALE:
2 = 0.20 ms/cm
V = 10 mv/cm for -40° C
V = 20 mv/cm for all others



military applications

The most recent type of Microstack, developed for military aerospace applications, is designed to meet the most rugged military and N.A.S.A. requirements while still providing low cost and important size and weight advantages. These military Microstacks can be designed to operate reliably in extremes of temperature, humidity, altitude, vibration shock and corrosive environments. They also include internal heat sinking for temperature equalization throughout the stack.

In addition they offer simplified servicing and ease of expansion.

IGC's quality training program includes a N.A.S.A. approved school for reliable hand soldering.

The Microstack concept is available as a solution to specific design problems through the use of IGC's Memory Stack Engineering Department. No matter what your needs, the chances are that the Microstack is your answer.

IGC MILITARY MICROSTACKS
are available to meet
military specifications including:

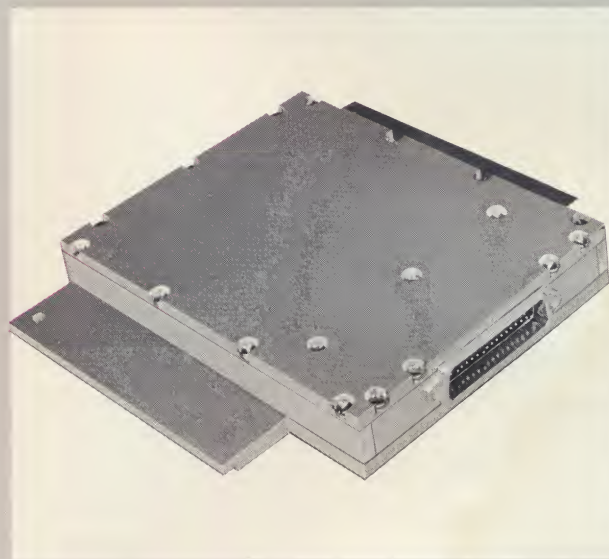
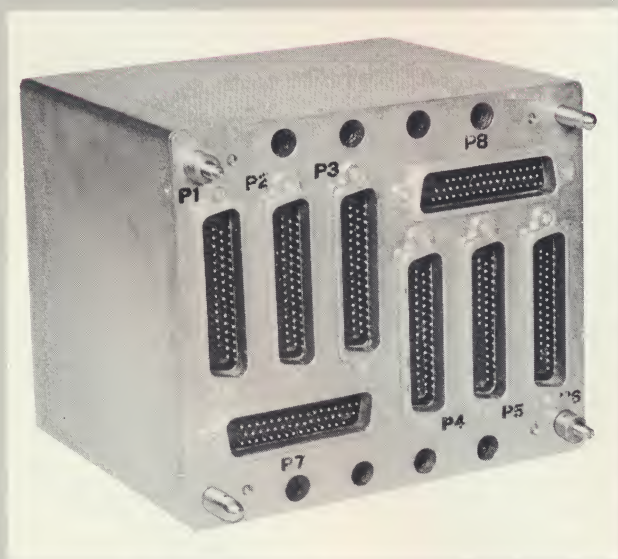
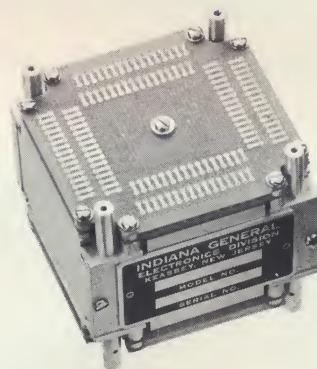
N.A.S.A. — NPC-200-3

Mil. — Q-9858A

Mil. — R-27542A

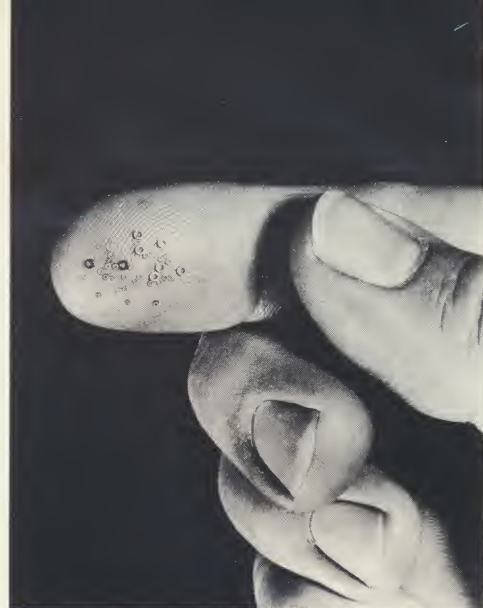
Mil. — E-5400

Typical Military Microstacks:
Upper Right 64 x 64 x 18;
Lower Left 32 x 64 x 40;
Lower Right 8 x 8 x 6.



typical mechanical parameters

TYPE OF STACK	Standard Microstack	Pluggable Microstack	Ground Support	Air Borne	Space Borne
SIZE AND CORE	66x64x8, 50 Mil Core	64x64x10, 50 Mil Core	32x64x48, 50 Mil Core	64x64x24, 30 Mil Core	64x64x18, 30 Mil Core
MECH. SIZE	4.75x4.75x1.19 26.9 cu. in.	4.75x4.75x1.84 41.5 cu. in.	6.3x5.5x5.3 167 cu. in.	2.94x2.94x2.69 23.2 cu. in.	3.19x3.00x2.39 23 cu. in.
FEATURES	Stacks may be added by pinning and soldering. External wires attached by customer to printed circuit	Integral connectors. Stacks may be added by plugging together. Ext. wires attached by customer to mating connectors furnished by IGC.	Built-in connectors. Mat mounting on copper plates. Customer makes connection with his mating connectors. Stack is 'open' permitting air flow through stack.	Integral Diode Matrix Boards. Mat mounted on tin plated surface of P.C. Boards. Integral Temp. Sensing series of Diodes. Sense and Inhibit External wires are furnished attached to stack. Customer solders drive line to Cambion terminals on stack.	Mat mounted on thin aluminum sheet. Each mat has two sections: DRO (Destructive read out) and NDRO (Nondestructive read out). Heat flow path provided to exterior of stack and to heat sink.
Weight/Power	.62lbs.		5.4 watts	1.11 lb. 3 watt	1.21 lbs. 3 watt Operational.
TEMPERATURES Operating		—50°C to +125°C (any 100°C range)	0°C to +52°C	—55°C to 125°C	—35°C. to +100°C
Non-Operating Spec. Ref.			—62°C to +71°C MIL-E-4158C, 2. 3. 281 MIL-E-4970A, 3. 1. 1. 2	—62°C to +125°C	—55°C to +100°C
TEMPERATURE SHOCK Operating				1.5°C per minute to +125°C —55°C to +100°C. Mil. Std.—202, Method 102A, MIL-STD-202B, Method 102A Test Cond. C. 7½ hrs. 5 cycles—1½ hrs. ea.	—55°C and +100°C 5 cycles, 1½ hours each
Non-operating					
VIBRATION Sinusoidal	May be shipped by any commercial carrier	MIL-E-5272C Proc. XII	5 to 300 cps/0.4" D.A. Max./20G max.	5 to 500 cps/0.2" D.A. Max/12G max. MIL-STD-202B, Method 204A, Test Cond. A Modified	OPERATING 5 cps @ 1.5G to 2000 cps @ 13Gs OPERATING 20 cps. to 2,000 cps. power spectral density .070 and .133 g ² /cps.
Random					
SHOCK Impact		10G	100G	50G MIL-STD-202B, Method 202A	OPERATING 15G
Table drop test					
MOISTURE RESISTANCE Non-operating		MIL-T-5422E Par. 4.4	95% Relative Humidity 21°C to 65°C 10 cycles 24 hr. each— MIL-E-4158C, 3.2.28 .1	90-98% Hum. Uncl. Condensation & Frost —10°C to +65°C to 10 cycles 24 hrs. each— MIL-STD-202B, Method 106B	0-100% Humidity 10 cycles 24 hrs. each MIL-STD-810A, Method 507
ALTITUDE Operating Non-operating		MIL-E-5272 Cond. C.	10,000 ft. 40,000 ft. MIL-F-4158C	70,000 ft. (1.31 inHg) MIL-STD-202, Method 105C, Test Cond. C.	OPERATING +100°C at 10 ⁻⁶ mmHg —35°C at 10 ⁻⁶ mmHg
SALT SPRAY/SALT FOG				48 hrs. MIL-STD-202, Method 101B, Test Cond. B	48 hrs. MIL-STD-810A, Method 509
SAND AND DUST					MIL-STD-801A, Method 510
GENERAL SPEC:			MIL-E-4158C MIL-E-4970A	MIL-E-5400 (ASG) MIL-T-5422E (ASG)	MIL-E-16400C MIL-E-4158
SPECIAL REQUIREMENTS				5-24cps 0.2" Test cond. A 24-50 6G 10-50—0.0G 50-500—10G 50-100 8G 100-250 12G 250-500 4G	Outgassing spec. less than 10 ⁻⁹ lbs./sec. at 100° C and 10 ⁻⁵ torr. after 72 hrs. NASA—NPC200-3
RELIABILITY			100,000 hours	100,000 hours	150,000 hours



IGC has the core you need . . . at its finger tips.

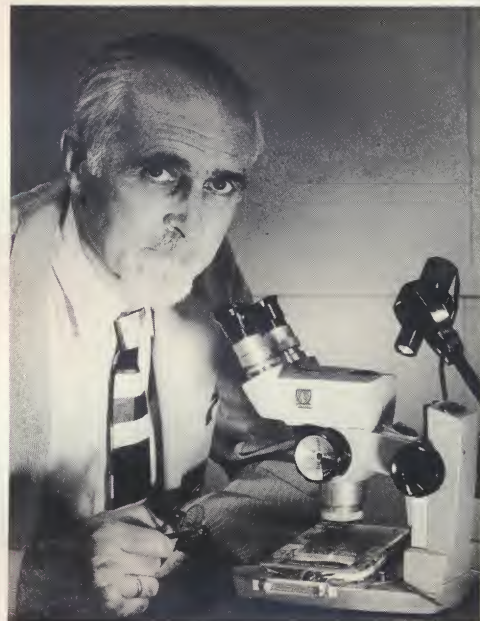
IGC

ferramic[®] memory cores

All three types of Microstacks are strung with Indiana General Ferramic memory cores. IGC's range of cores is one of the most extensive in the industry with a complete selection of conventional and wide-temperature cores for speeds down to 200 nanoseconds in 30, 50, and 80 mil sizes. Techniques for the use of IGC 20 mil Cores in Microstacks are presently under development.

Indiana General's extensive background in core design and manufacturing, which dates back to our invention and patenting of the square loop ferrite, is a further benefit to the designer. Our engineering department is available to help in selecting the optimum core for your application. Core production capacity, and guaranteed repeatability are further IGC advantages assuring quality stacks and on-time delivery.

A complete file of engineering data sheets, listing specifications and operational data is available for IGC's full line of Ferramic memory cores.



IGC scientists, led by Dr. Ernst Albers-Schoenberg, invented the square-loop ferrite memory core and today practically every manufacturer of memory devices or computers uses cores made or licensed by IGC.

INDIANA GENERAL

ELECTRONICS DIVISION / MEMORY PRODUCTS
KEASBEY, NEW JERSEY

COMMERCIAL MICROSTACK®

Typical Operational Data

Core Size = 50 Mil (MC-138) • Sense Load = 100 ohms • Tr = 0.5 μ seconds • Td = 3.0 μ seconds • Pulse Repetition Rate = 10 k. c. • Read, Write cycle time = 10 μ seconds • Pattern = Double checkerboard "worst noise condition" • Inhibit Current = -10% of "Y" current
2

MICROSTACK SIZE	64 x 64 x 8			32 x 32 x 8			16 x 16 x 8			10 x 10 x 8		
Current in milliamperes	450	500	550	450	500	550	450	500	550	450	500	550
Minimum "1" millivolts	35	45	52	40	49	54	44	54	64	44	53	64
Maximum "0" millivolts	11	12	13	6	5	9	4	5	4	8	8	8
Tp	0.90	0.85	0.80	0.90	0.85	0.80	0.85	0.80	0.78	0.85	0.80	0.78
Ts	1.80	1.70	1.60	1.75	1.65	1.60	1.65	1.55	1.50	1.60	1.55	1.50
Tp'	0.80	0.70	0.60	0.60	0.50	0.50	0.50	0.45	0.40	0.55	0.48	0.43
Ts'	1.70	1.55	1.40	1.40	1.25	1.20	1.40	1.20	1.10	1.40	1.24	1.12

Typical Values

MICROSTACK SIZE	64 x 64 x 8			32 x 32 x 8			16 x 16 x 8			10 x 10 x 8		
Eac of "X" Drive Line	1.80	2.00	2.20	1.00	1.05	1.20	0.75	0.78	0.80	0.53	0.64	0.74
Eac of "Xn" Drive Line	1.70	1.90	2.10	0.88	0.98	1.30	0.60	0.66	0.80	0.50	0.61	0.70
Eac of "Y" Drive Line	1.40	1.50	1.60	0.58	0.76	0.92	0.58	0.63	0.73	0.50	0.61	0.71
Eac of Inhibit Line	7.80	8.00	8.20	1.80	1.90	2.20	0.38	0.41	0.44	0.25	0.27	0.29
*Luh of "X" Drive Line	3.20			1.44			1.25			1.02		
Luh of "Y" Drive Line	2.40			1.22			1.01			0.97		
Luh of Inhibit Line	16.00			3.80			0.82			0.54		
R of "X" Drive Line	3.20			1.53			0.86			0.56		
R of "Y" Drive Line	1.79			0.90			0.50			0.37		
R of Inhibit Line	12.60			3.87			1.04			0.56		
R of Sense Line	18.56			5.00			1.40			0.70		

*Inductance calculated at nominal drive current for all cases.

Typical Operational Data

Core Size = 50 Mil (MC-140) • Sense Load = 100 ohms • Tr = 0.5 μ seconds • Td = 3.0 μ seconds • Pulse Repetition Rate = 10 k. c. • Read, Write cycle time = 10 μ seconds • Pattern = Double checkerboard "worst noise condition" • Inhibit Current = -10% of "Y" current
2

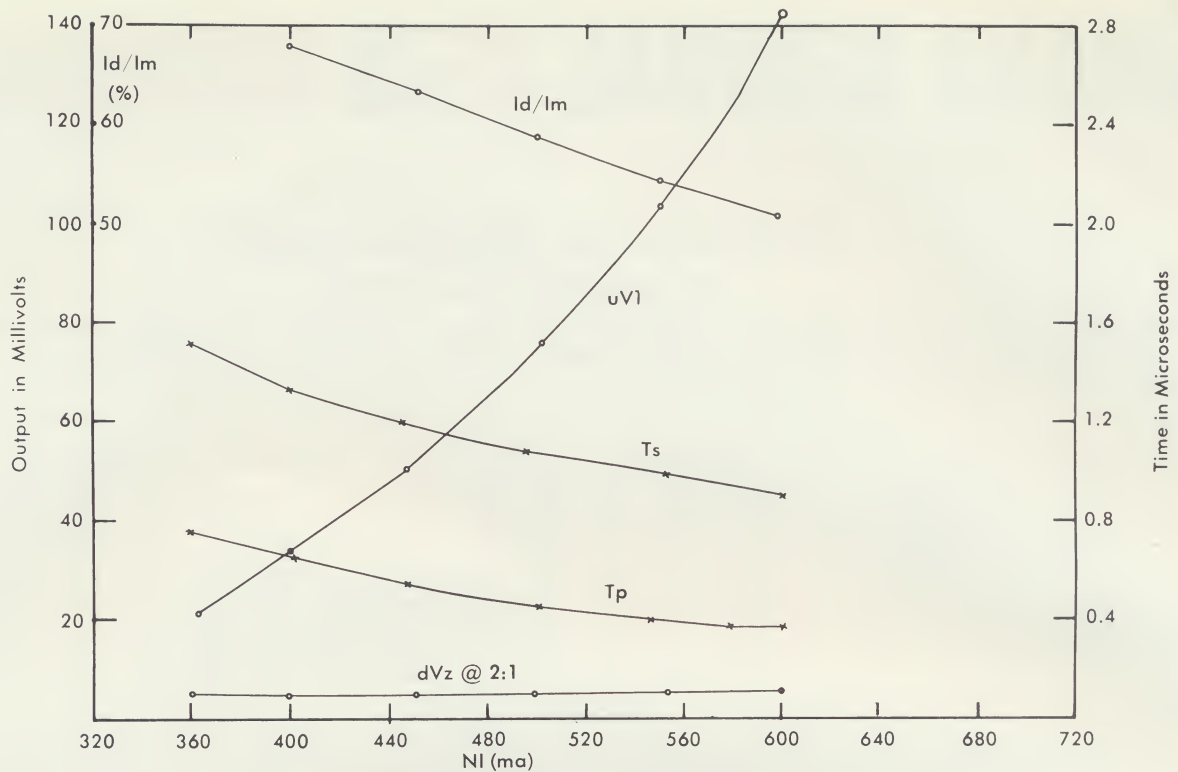
MICROSTACK SIZE	64 x 64 x 8			32 x 32 x 8			16 x 16 x 8			10 x 10 x 8		
Current in milliamperes	380	420	460	380	420	460	380	420	460	380	420	460
Minimum "1" millivolts	36	43	50	38	48	56	42	52	61	42	54	62
Maximum "0" millivolts	11	12	13	8	8	8	4	4	5	7	7.5	7
Tp	1.00	0.90	0.85	0.95	0.84	0.80	0.85	0.80	0.75	0.88	0.81	0.74
Ts	1.90	1.80	1.65	1.70	1.60	1.50	1.70	1.60	1.45	1.70	1.60	1.44
Tp'	0.80	0.70	0.65	0.70	0.60	0.55	0.58	0.50	0.50	0.60	0.48	0.44
Ts'	1.70	1.55	1.45	1.55	1.40	1.25	1.45	1.30	1.20	1.40	1.24	1.16

Typical Values

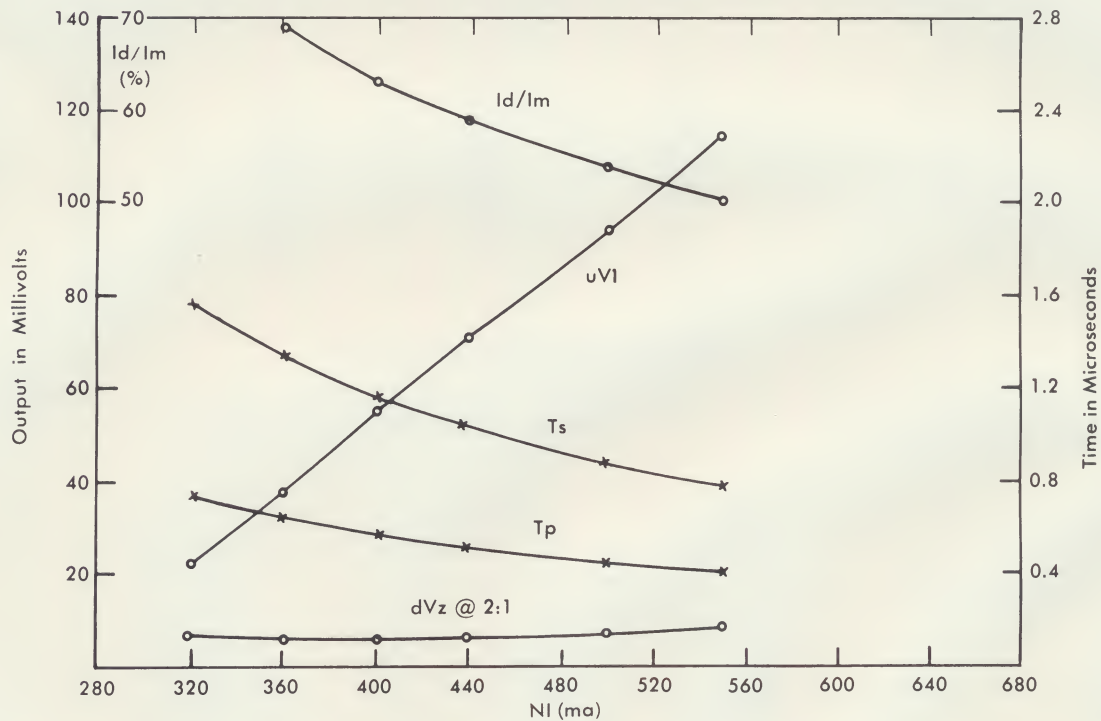
MICROSTACK SIZE	64 x 64 x 8			32 x 32 x 8			16 x 16 x 8			10 x 10 x 8		
Eac of "X" Drive Line	1.60	1.65	1.80	0.88	0.96	1.00	0.52	0.64	0.70	0.50	0.60	0.72
Eac of "Xn" Drive Line	1.50	1.60	1.70	0.84	0.90	1.00	0.50	0.64	0.74	0.50	0.60	0.72
Eac of "Y" Drive Line	1.30	1.35	1.50	0.68	0.70	0.80	0.45	0.60	0.75	0.48	0.56	0.68
Eac of Inhibit Line	8.00	8.20	8.40	1.70	1.80	1.90	0.43	0.51	0.54	0.21	0.23	0.25
*Luh of "X" Drive Line	3.14			1.84			1.2			1.12		
Luh of "Y" Drive Line	2.65			1.68			1.12			1.06		
Luh of Inhibit Line	17.2			3.76			1.07			0.48		
R of "X" Drive Line	3.07			1.60			0.85			0.42		
R of "Y" Drive Line	1.80			0.95			0.53			0.40		
R of Inhibit Line	12.80			3.40			1.10			0.60		
R of Sense Line	18.00			4.70			1.50			0.54		

*Inductance calculated at nominal drive current for all cases.

MC-138



MC-140



Key

- T_r — Rise time of current pulse measured from 10% of 90% of leading edge.
- T_d — Pulse duration, measured from 90% to 90% of flat top portion of current pulse.
- T_p — Peak time of core outputs appearing across sense winding, referenced to 10% point of leading edge of current pulse.
- $T_{p'}$ — Peak time of core outputs appearing across sense winding, referenced to 10% point of core outputs.

- T_s — Switch time of core outputs appearing across sense winding, referenced to 10% point of leading edge current pulse.
- $T_{s'}$ — Switch time of core outputs appearing across sense winding, referenced to 10% point of core outputs.
- R — Resistance in ohms.
- E_{ac} — Peak voltage developed across memory plane.